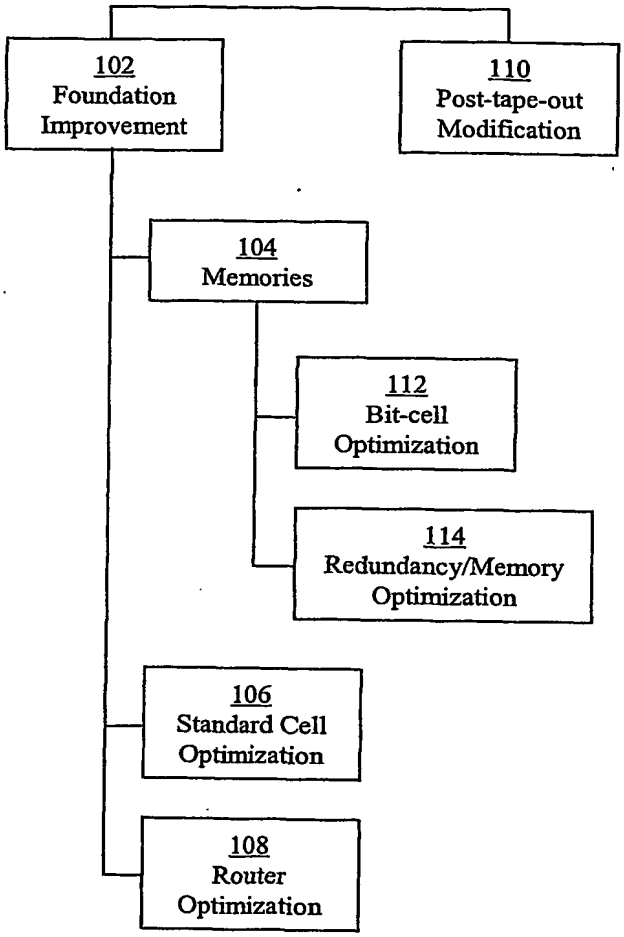

FIG. 1: Taxonomy of Design Based Yield Improvements

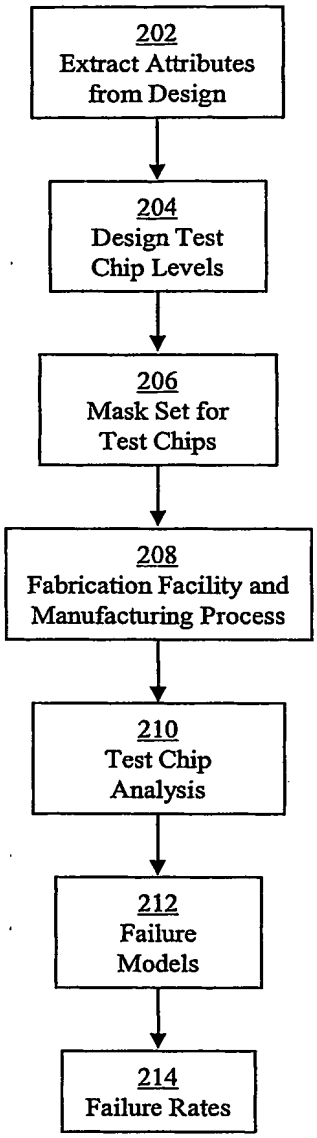

FIG. 2: Determining "Existing Failure Models"

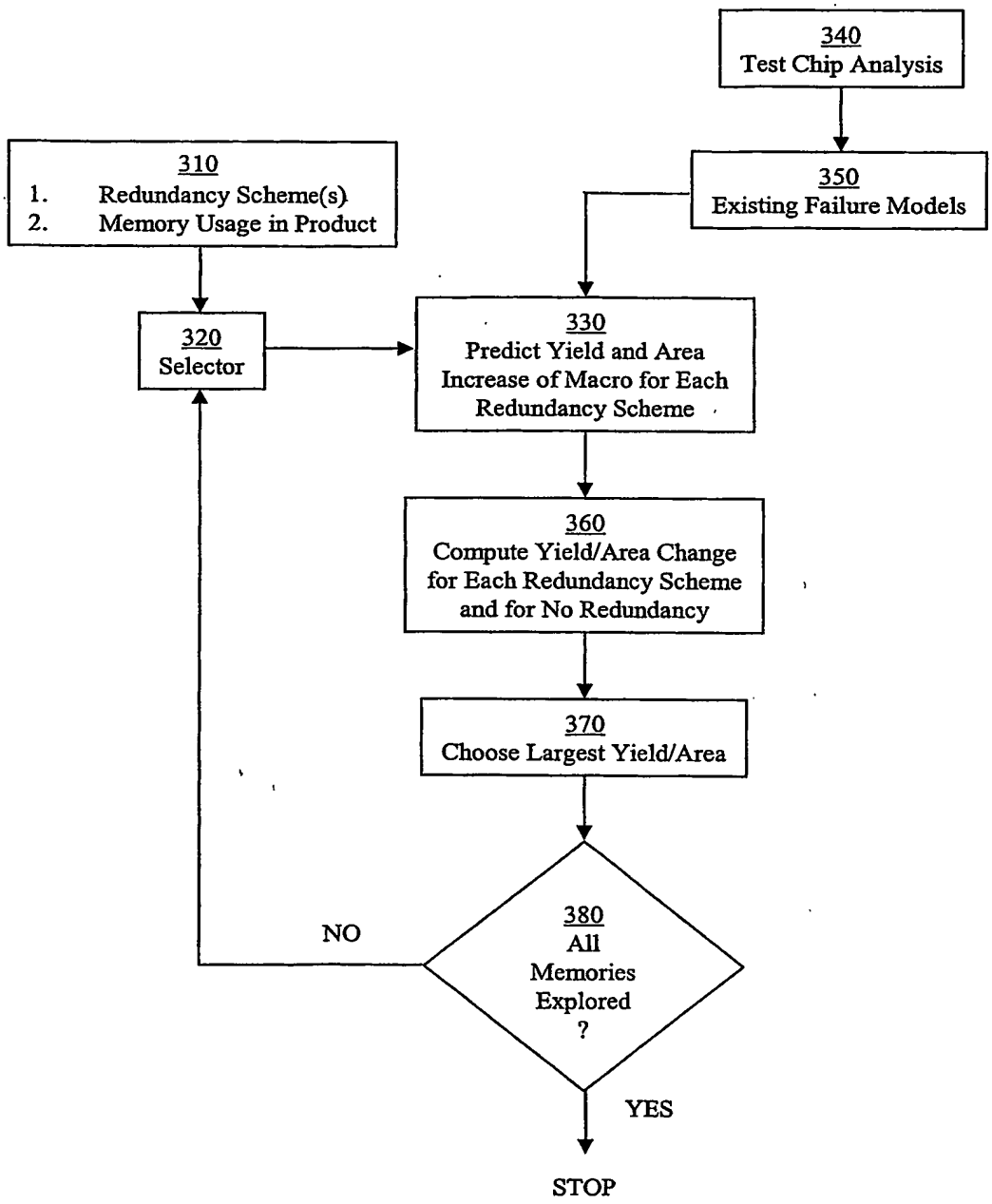

FIG. 3: Bit-Cell Optimization

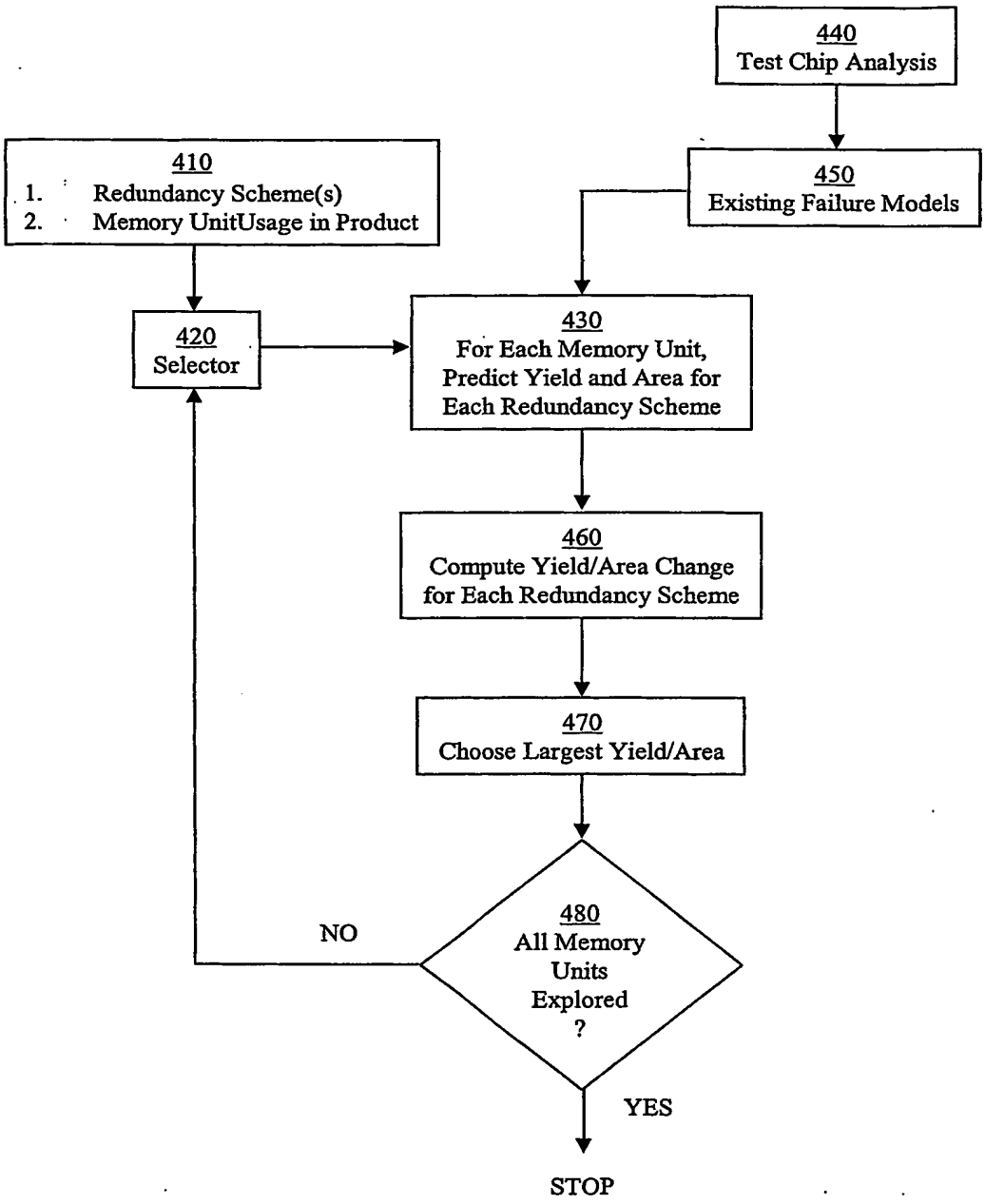

FIG. 4: Redundancy Optimization

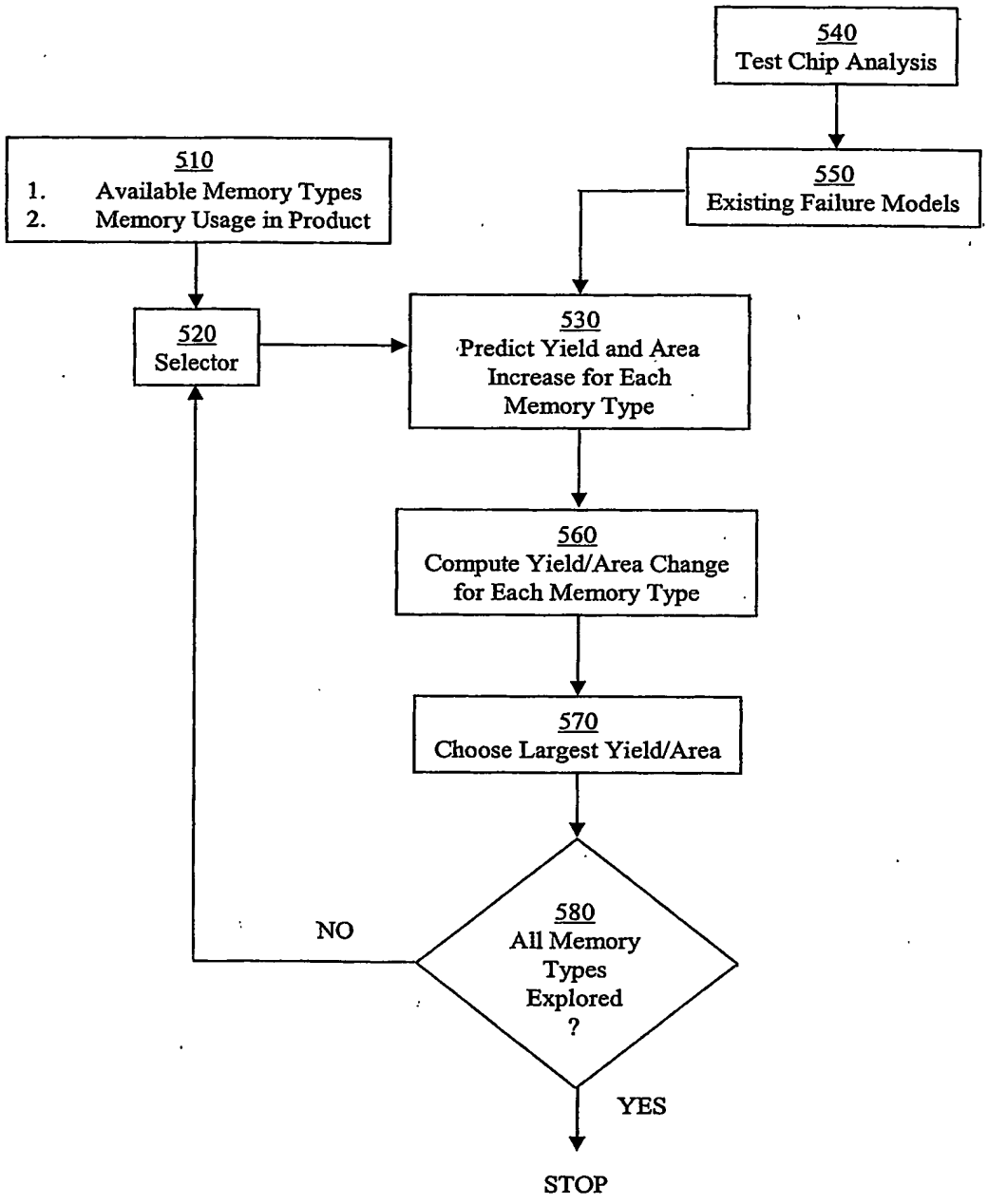

FIG. 5: Memory Type Optimization

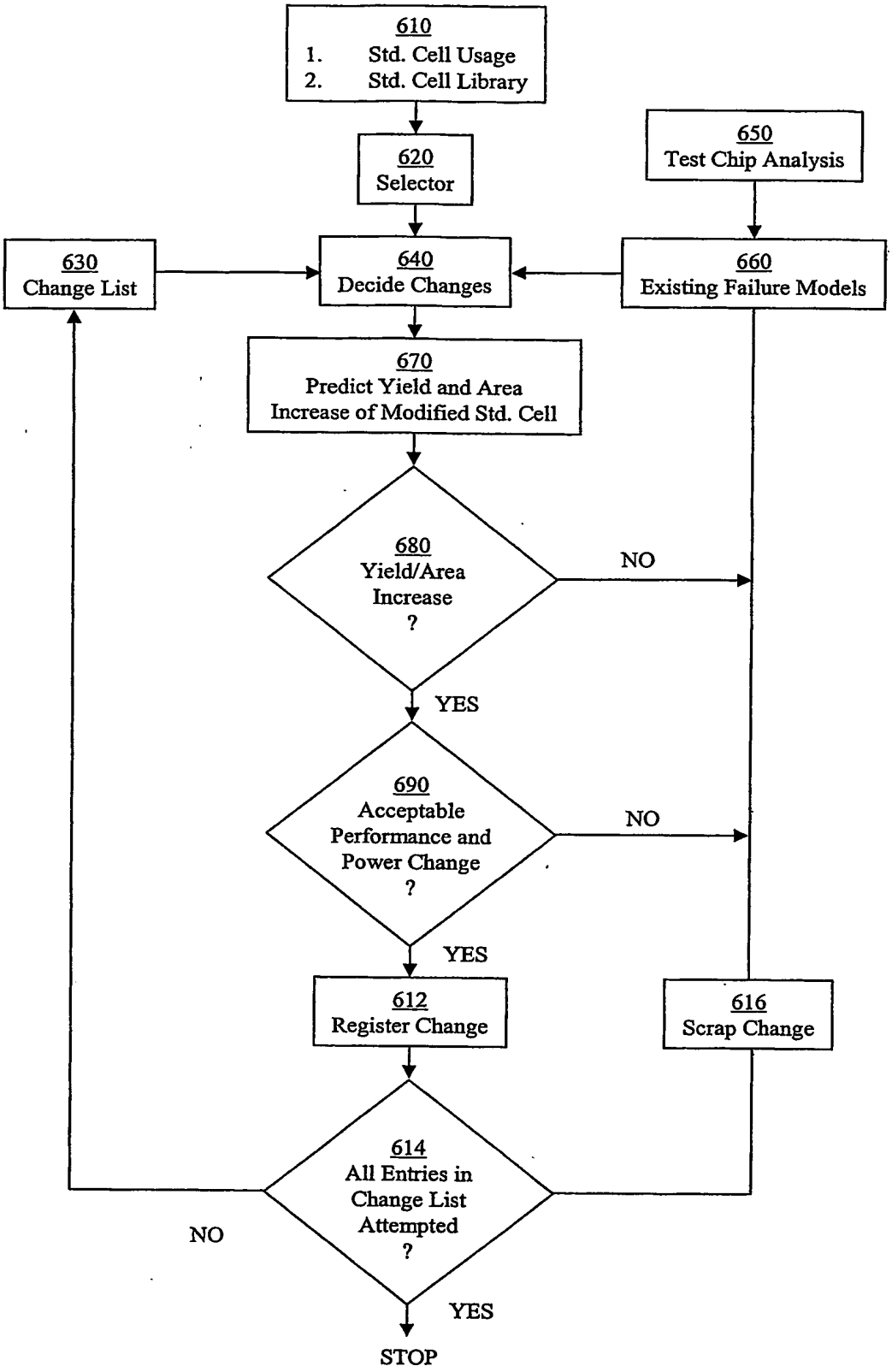

FIG. 6: Standard Cell Optimization

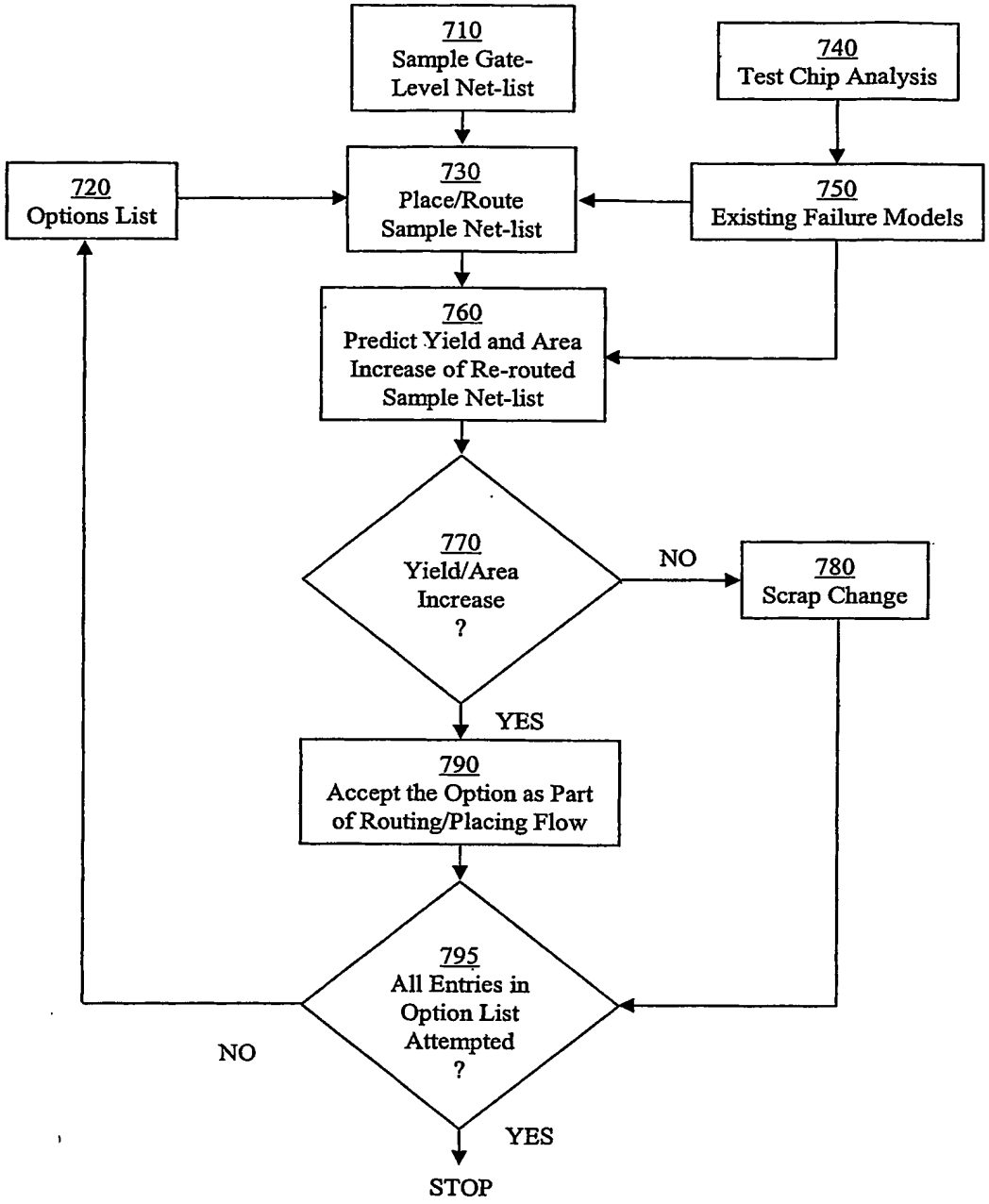

FIG. 7: Router Optimization

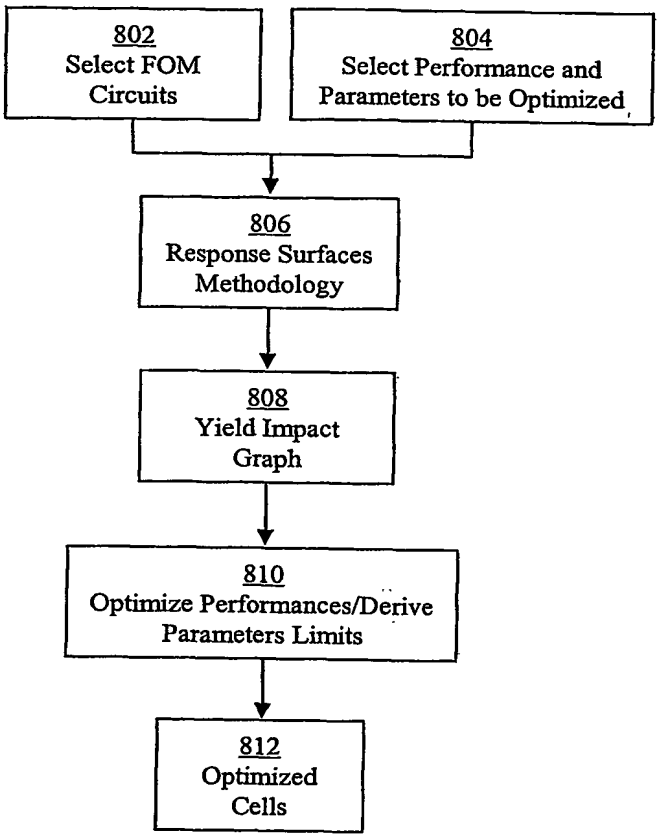

FIG. 8: Parametric Yield Optimization

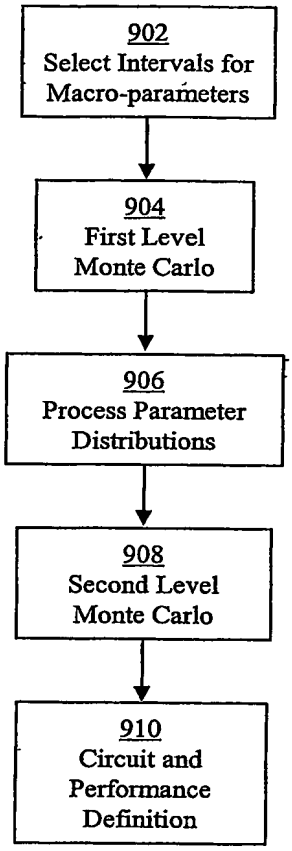

FIG. 9: Yield Impact Graph

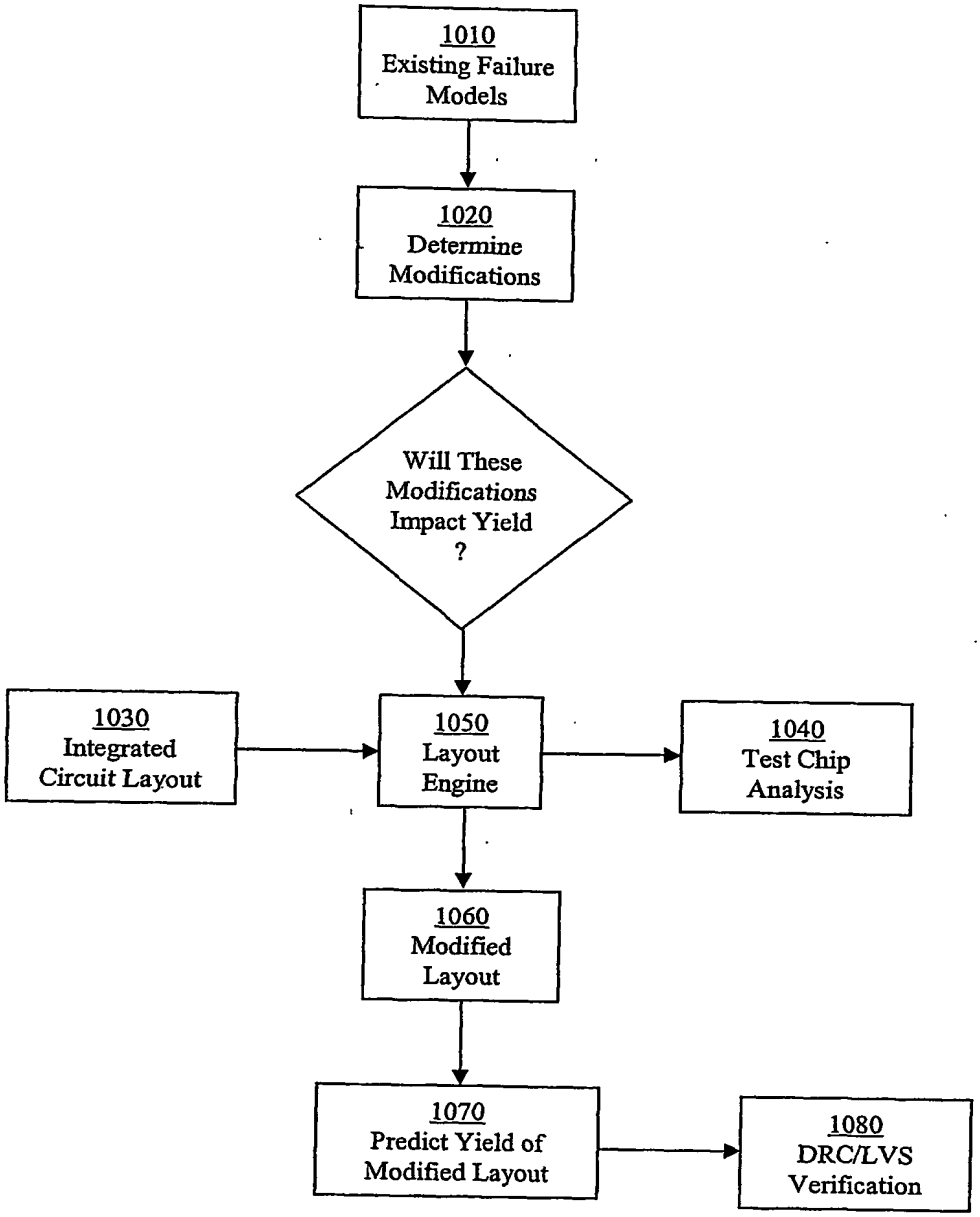

FIG. 10: Post-tape-out Modification